A Monolithic 40 V/20 A GaN Half Bridge IC with Integrated Gate Drivers and Level-shifters

Öncü Benli Marin Palomo
MinDCet *NV*
Leuven, Belgium
oncu@mindcet.com

Jef Thone
MinDCet *NV*
Leuven, Belgium
jef@mindcet.com

Rana Asad Ali
Wurth Elektronik eiSos Group
Munich, Germany
ranaasad.ali@we-online.de

Mahmoud Shousha
Wurth Elektronik eiSos Group
Munich, Germany
mahmoud.shousha@we-online.de

Martin Haug
Wurth Elektronik eiSos Group
Munich, Germany
martin.haug@we-online.de

Olga Syshchyk
IMEC
Leuven, Belgium
olga.syshchyk@imec.be

Matteo Borga
IMEC
Leuven, Belgium
matteo.borga@imec.be

Stefaan Decoutere
IMEC
Leuven, Belgium
stefaan.decoutere@imec.be

Marc Fossion
Thales Alenia Space
Charleroi, Belgium
marc.fossion@thalesalenia space.com

Tuan-Dat Mai
Thales Alenia Space
Charleroi, Belgium
tuandat.mai@thalesalenia space.com

Mike Wens
MinDCet NV
Leuven, Belgium
mike@mindcet.com

***Abstract*— 40 V-rated half-bridges are realized in 100 V Gallium-Nitride on Silicon (GaN-on-Si) and 100 V Gallium-Nitride on Silicon-on-Insulator (GaN-on-SOI) technologies from IMEC. Electrical characterization is done to investigate several key parameters such as on-resistance, gate and drain leakage, and output capacitance. The performance of GaN-on-Si and GaN-on-SOI technologies are compared. In addition, step-stress testing and key parameter drift analysis are performed on the GaN-on-Si half-bridges. Furthermore, a monolithic 40 V/20 A half-bridge with integrated gate drivers, level shifters, floating supplies, and dead time controller circuitry is realized in 100 V GaN-on-Si technology as a part of a point-of-load (PoL) converter achieving 80 % efficiency and reaching an integrated solution with IC active area of 44.15 mm² which is 35 % smaller compared to state-of-the-art commercial integrated solutions. Functionality tests are performed for integrated monolithic half-bridge chips. Finally, further testing is done on a system-level Si-GaN hybrid PoL converter.**

Keywords—Gallium-Nitride, half-bridge, power electronics, wide bandgap, monolithic integration

I. INTRODUCTION

Gallium Nitride (GaN) became particularly valuable in power electronics due to improved figures of merit compared to Silicon (Si) counterparts. On-resistance, breakdown voltage, and switching efficiency are part of the relevant characteristics of the technology [1]. For example, the switching figure of merit ($Q_{Gate} \times R_{DS,on}$) makes the GaN transistor an advantageous choice for high-efficiency high-frequency power electronics. Concurrently, high switching frequencies enable the use of smaller passives, effectively reducing the total system size. In reality, GaN power stages with external gate drivers come with inherent and unwanted parasitics such as PCB track and bond wire inductances. These parasitics can be destructive in combination with high switching frequencies and effectively limit the maximal operating frequency. This problem can be solved by increasing the integration level and moving towards monolithic chips. Integrated gate drivers help to mitigate this problem by being physically closer to the gate and therefore having fewer parasitics.

This work was supported by the European Commission, the project is part of the EU-funded GaN Transistor Integrated Circuits project EleGaNT — SPACE-10-TEC-2018-2020.

The research documented in this paper illustrates half-bridge chips realized in GaN-on-Si and GaN-on-Silicon-on-Insulator (GaN-on-SOI). These half-bridge ICs are characterized while comparing the impact of the two technologies. In addition, step stress testing is done to check how the relevant transistor parameters change due to stress over time. Furthermore, in this paper, we describe a monolithic 40 V/20 A half bridge with all required periphery: integrated gate drivers, level shifters, and dead time control.

The paper is structured as follows: The technology overview is presented in Section II introducing 100 V-rated GaN-on-Si and GaN-on-SOI technologies of IMEC. The design overview is given in Section III focusing on the monolithic half-bridge chip. The packaging aspect is treated in Section IV. The characterization results can be found in Section V. Finally, a more thorough application-oriented Si-GaN hybrid point-of-load converter is presented in Section VI.

II. TECHNOLOGY

Monolithically integrated circuits are fabricated using 900 µm thick 200 mm Si and SOI substrates with a 1.5 µm SiO_2 buried layer, and a 1.5 µm Si (111) top layer. The epitaxial stack with a total thickness of less than 2 µm was grown using metalorganic chemical vapor deposition (MOCVD). Epitaxial stacks, channel thickness, AlGaN barrier thickness, composition and Mg doping are similar to what is used in imec's discrete p-GaN gate E-mode GaN power devices on GaN-on-Si substrates [2].

Fig.1 shows a schematic cross-section and TEM (transmission electron microscopy) image of the fabricated p-GaN gate HEMTs. The ICs fabrication starts with the simultaneous p-GaN gate and gate metal patterning, followed by the deposition of a thin surface passivation dielectric. Further processing includes the formation of source and drain ohmic contacts. A Ti/Al/TiN - based stack is used for ohmic contact formation using a low temperature anneal. The technology has a fully planarized backend with two Al-based interconnect levels and W- plugs connections. PECVD SiO_2 layers are used as inter metal dielectrics and a Si_3N_4

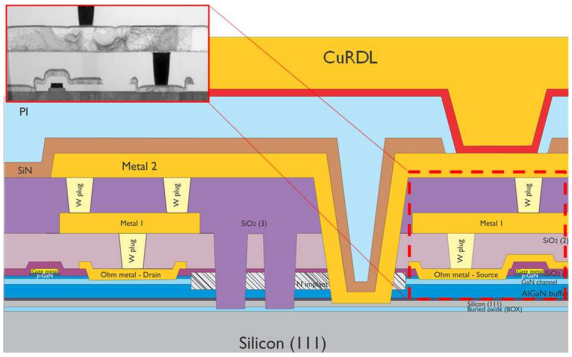

Fig. 1. Schematics of the E-mode pGaN HEMTs using GaN-on-SOI technology with cross-section TEM images of the processed devices.

passivation is deposited on top of the second metal level. Finally, a polyimide layer and a thick Cu plated redistribution layer (Cu-RDL) are processed. To ensure isolation between high-side and low-side, GaN-on-SOI offers a solution with deep trench isolation (DTI) down to the buried oxide layer and connecting the thin Si layer with the sources of the power devices with a deep substrate contact. The isolating trenches help to avoid back-gating effects for the high-side HEMT during switching, and limit crosstalk between the power devices and the sensitive analog/logic areas of the GaN-IC. The p-GaN gate HEMT performance and reliability for power GaN-based technologies is described in several publications [3-5].

III. Design

The half-bridge chip consists of two n-type enhancement-mode 40 V-rated GaN HEMTs. The metallization is designed considering the expected current densities for an output current capability of 20 A up to 125 °C. The total gate width of the low side HEMT is 840 mm and the high side HEMT total gate width is 420 mm. The asymmetrical sizing is chosen due to the low duty cycle nature of the Point-of-Load (PoL) converter application. Two versions of the half-bridge ICs are taped in GaN-on-Si and GaN-on-SOI.

The advanced monolithic half-bridge IC includes the same asymmetrical power stage. In addition, it features gate drivers, level shifters, and dead time control as shown in the block diagram in Fig. 2.

Thorough architecture and design choices were made considering the technology's constraints. The absence of p-type or depletion-type devices restricts the design options. Furthermore, circuit topologies not relying on well-matched devices were employed, due to threshold voltage mismatch in GaN being larger than in Si.

A. Dead Time Controller

The dead time controller generates two non-overlapping signals based on the input, pulse width modulation (PWM) signal. The output of the dead time controller travels to the low side and the high side level shifters.

The dead time between these two signals is configured by a delay element, which relies on an inverter charging a capacitor. The amount of capacitance can be programmed via a 3-bit digital signal called *tdead_control*.

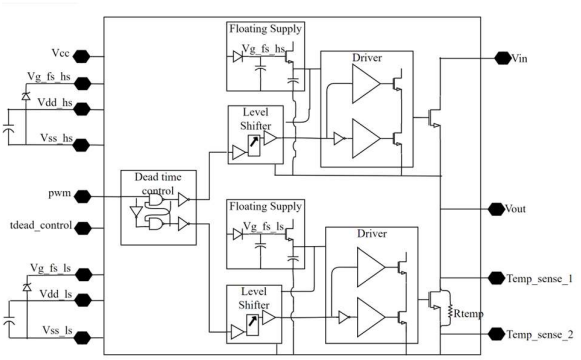

Fig. 2. Block diagram of the half-bridge IC with integrated drivers, level shifters, dead time control, and floating supply generation. The required external components (zener diodes and decoupling capacitors) are included in the drawing.

B. Level Shifter

The level shifter takes the input signal from the ground voltage domain and brings it to the high-side and the low-side floating voltage domain. Each floating voltage domain is referenced to the source of the power HEMT in the half-bridge.

Due to a lack of p-type devices, the up level shifting is done via resistors followed by a set-reset (SR) NOR latch. The digital gates are implemented in Resistor Transistor Logic (RTL). In this block, a trade-off is made between speed and power density.

C. Gate Driver

This design has two gate drivers, one for the high-side and one for the low-side power HEMT in the half-bridge configuration. Each gate driver operates in its respective floating voltage domain referenced to the source of the power HEMTs in the half-bridge. Dedicated floating supply blocks generate the floating voltages.

D. Floating Supply

A 100 V-rated HEMT is used in a source follower configuration, to buffer the supply voltage in combination with on-chip and external decoupling capacitors. There is an integrated bootstrap circuit that utilizes an on-chip diode connected 100 V-rated HEMT and an external capacitor.

IV. Packaging

The embedding of power devices into PCBs has been used in the power electronics fields for more than a dozen years. It offers many advantages compared to the conventional ones by reducing size and optimizing the interconnections resulting in increased power density, reduced parasitic inductance, and better thermal management [6].

A core achievement in die packaging for space applications was the move from conventional wire bonding to advanced PCB-embedded technology. The GaN-on-Si and GaN-on-SOI were embedded inside High Tg FR4 using a micro via manufacturing process. The semiconductor was first assembled face down on copper foil with non-conductive adhesive and embedded by a multilayer pressing process. Then, laser drilling and copper metallization enabled a direct electrical connection between the chip top side metallization

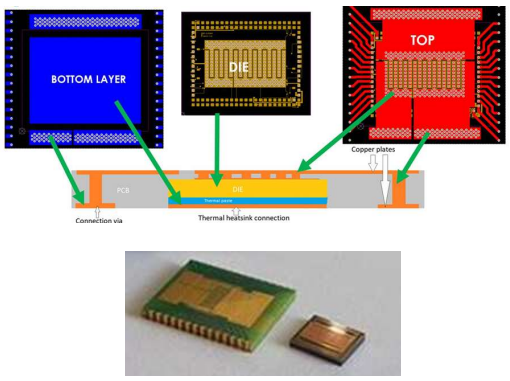

Fig. 3. Schematic cross-section of embedded device (top) and manufactured prototype compared with initial dice (bottom).

and PCB. Fig. 3 shows the schematic cross-section of the embedded device and the manufactured prototypes.

V. Characterization

Characterization of the GaN-on-Si and GaN-on-SOI half-bridge ICs is done where on-resistance, threshold voltage, gate and drain leakage, and output capacitance are measured. The half-bridge chips are wire bonded allowing four-wire measurements on the drain and source sense connections.

The threshold voltage is measured by sweeping the gate to source voltage V_{gs} from 0 to 6 V in 100 mV steps. For each V_{gs} value, a 5 mV pulse of drain to source voltage V_{ds} is applied and drain to source current I_{ds} is measured. The threshold voltage is calculated by

$$V_{th} = V_{gs} - V_{ds}/2 \quad (1)$$

when I_{ds} is zero. The corresponding V_{gs} value is determined by fitting a line on the I_{ds}-V_{gs} plot and calculating the zero crossing.

The on-resistance is measured for a V_{gs} of 6 V and by forcing I_{ds} pulses in a range of 10 mA to 1A and measuring the V_{ds} volType equation here.tage. The on-resistance $R_{ds,on}$ is defined by

$$R_{ds,on} = V_{ds}/I_{ds}. \quad (2)$$

The gate leakage is measured when V_{ds} is forced to 0 V and the V_{gs} voltage is varied from 0 to 6 V in steps of 100 mV. The gate to source I_{gs} current is monitored.

The drain leakage measurements are done when V_{gs} is 0 V, and V_{ds} is swept from 0 to 40 V in 1 V steps and the I_{ds} is measured.

The output capacitance C_{oss} is measured by using the equation

$$C_{oss} = \frac{V_{bus}\, I_{bus}}{f V_{bus}^2}. \quad (3)$$

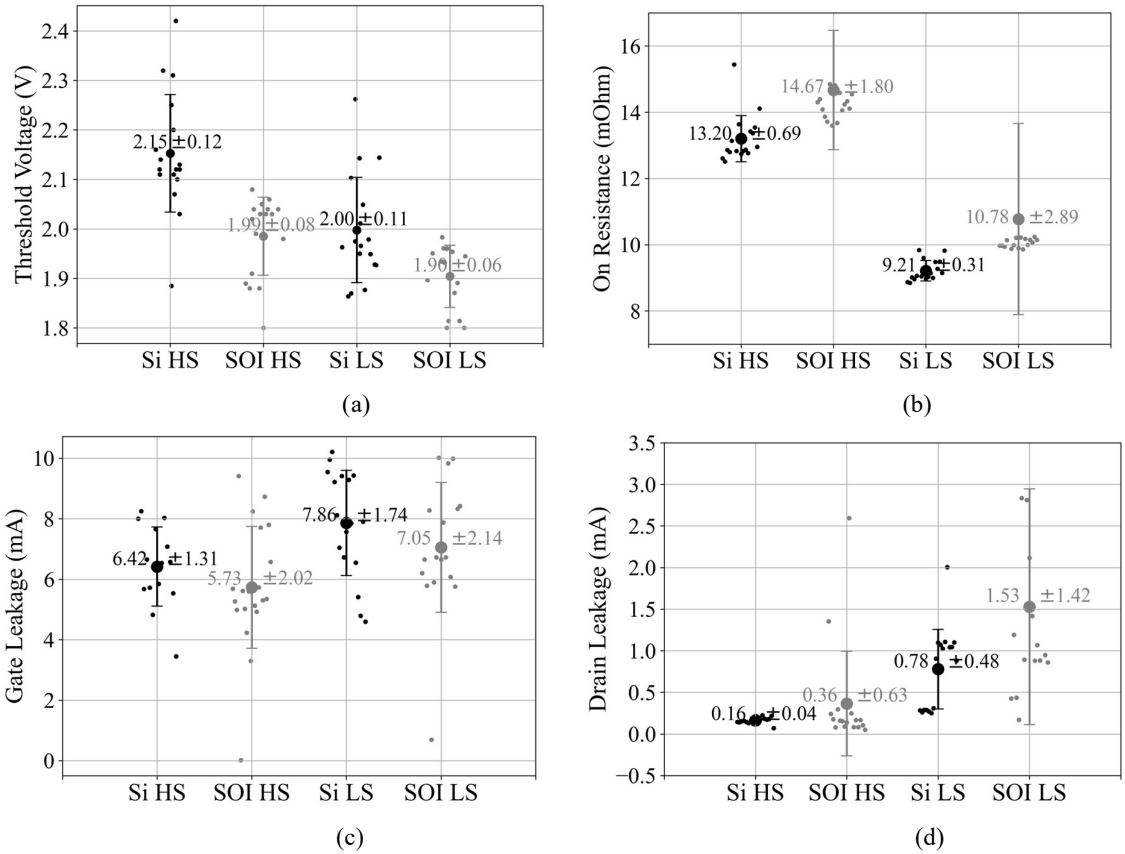

Fig. 4. Characterization plots showing (a) threshold values, (b) on-resistance, (c) gate leakage current, and (d) drain leakage current for high side (HS) and low side (LS) HEMTs in the half bridges manufactured using GaN on Si and GaN on SOI technologies. Mean and standard deviation values are denoted on the graphs.

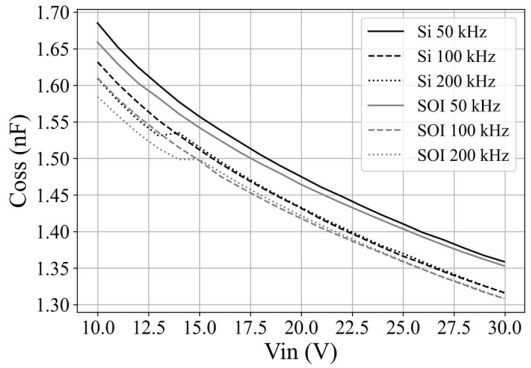

Fig. 5. Output capacitance versus input voltage for GaN-on-Si and GaN-on-SOI samples at input frequencies of 50 kHz, 100 kHz and 200 kHz.

The characterization result overview is presented in Fig. 4 and Fig. 5. The results are based on 17 GaN-on-Si and 17 GaN-on-SOI half-bridge samples. The measured median threshold values are between 1.9 V and 2.2 V considering HS and LS, on both GaN-on-Si and GaN-on-SOI. Within the GaN-on-Si samples, there is a small variation of 0.12 V, whereas this is 0.08 V on GaN-on-SOI samples. These values fall into the simulated worst power corner case and are therefore considered insignificant. The mean value of the on-resistance is about 1 mOhm lower for GaN-on-Si samples as well as showing less deviation compared to GaN-on-SOI samples, possibly due to differences in the epitaxial layer properties. The gate leakage of the GaN-on-SOI and GaN-on-Si samples is comparable with GaN-on-SOI showing 0.7 mA lower leakage than its GaN-on-Si counterpart. On the other hand, the off-state drain leakage of GaN-on-SOI samples is slightly higher than the GaN-on-Si samples. In the leakage plots shown in Fig. 4. (c) and (d), the drain leakage values are noted for V_{ds} of 32 V and the gate leakage values for V_{gs} of 5.6 V.

The output capacitance C_{oss} results shown in Fig. 5 originate from a GaN-on-Si and a GaN-on-SOI sample to represent the general behavior. The C_{oss} of the half-bridge is measured for various input voltage values from 10 V to 30 V and frequencies of 50 kHz, 100 kHz, and 200 kHz. The GaN-on-Si samples have a similar Coss to GaN-on-SOI samples with GaN-on-Si samples showing a 3 % larger C_{oss} compared to their GaN-on-SOI counterparts.

Following the general characterization, two types of step stress testing are done: drain-to-source V_{ds} and gate-to-source V_{gs} step stress test. These tests are performed on the high-side HS and low-side LS power HEMTs of the half-bridge chips in GaN-on-Si technology.

In the V_{ds} step stress test, 95 %, 100 %, 105 %, 110 %, 120 %, and again 120 % of the maximum rated drain-to-source voltage is applied while the gate-to-source voltage is 0 V, for 48 hours. The maximum drain-to-source voltage rating of the tested power HEMTs is 40 V. This corresponds to the following drain-to-source stress voltages 38 V, 40 V, 42 V, 44 V, and 48 V. The stressed samples are measured within 2 hours after each stress. When testing one of the power HEMT devices, the other one has gate and source, as well as drain and source pins, shorted.

In V_{gs} step stress testing, 95 %, 100 %, 105 %, 110 %, 120 %, and 120 % of the maximum rated gate voltage is applied when drain-to-source voltage is 0 V. The specified maximum gate voltage of the HEMTs is 7 V, corresponding to 6.65 V, 7 V, 7.35 V, 7.7 V, and 8.4 V gate stress voltages. The characterization of the HEMTs is done within 2 hours after each stress point. The results are summarized in Table 1 and Table 2.

TABLE I. THE NUMBER OF DAMAGED DEVICES AFTER STRESSING THEM WITH A CERTAIN PERCENTAGE OF THE MAXIMUM RATED DRAIN VOLTAGE. 15 HS AND 15 LS DEVICES ARE TESTED.

Test Type	Side	0 %	95 %	100 %	105 %	110 %	120 %	120 %
V_{ds} step stress	HS	1	2	2	2	3	3	3
	LS	1	1	1	1	1	1	1

TABLE II. THE NUMBER OF DAMAGED DEVICES AFTER STRESSING THEM WITH A CERTAIN PERCENTAGE OF THE MAXIMUM RATED GATE VOLTAGE. 15 HS AND 15 LS DEVICES ARE TESTED.

Test Type	Side	0 %	95 %	100 %	105 %	110 %	120 %	120 %
V_{gs} step stress	HS	0	2	2	3	5	14	15
	LS	0	0	3	4	7	15	15

4 devices out of 30 have failed in the V_{ds} step stress test. The main drifting parameter was the drain-to-source leakage current. It is observed for 13 out of 15 samples that the drain-to-source leakage current decreased on average 46.8 % at 120 % stress compared to its pristine value. A measurement from one of the samples is shown in Fig. 6 to visualize this behavior. The threshold voltage remained unchanged for undamaged devices indicating change in the leakage current is not caused by a threshold voltage drift.

During gate stress testing all devices failed at a maximum stress voltage of 8.4 V. Before getting damaged, their I_{ds} versus V_{gs} curves changed visibly with the threshold voltage increasing. Their on-resistance and leakage currents have consequently increased as well. Multiple HEMTs demonstrated less gate leakage in the subsequent stress measurement indicating a recovering behavior. This behavior is potentially linked to the electrostatic discharge (ESD) protection circuits located at the gate of the HEMTs. Detailed analysis of this behavior is outside the scope of this work.

The monolithic half-bridge chip with integrated gate drivers and level shifters is tested in a buck configuration as a PoL converter. It uses a 1.2 µH inductor with 0.42 mOhm Equivalent Series Resistance (ESR) and a 70 µF output capacitor. The transient measurements in Fig. 7 show the PoL converter operating at 400 kHz with a duty cycle of 16 %,

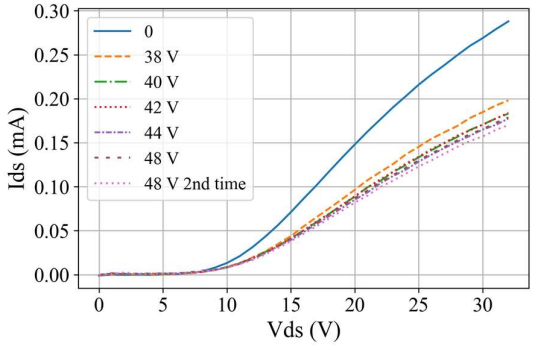

Fig. 6. Drain leakage current versus drain-to-source voltage after V_{ds} step stress testing.

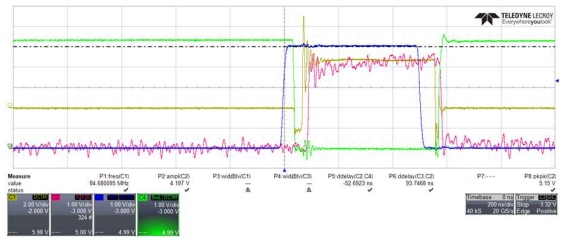

Fig. 7. The measured gate voltages of high side (blue line and red line for probe delay corrected version) and low side (green line) power HEMTs and output voltage (yellow line) from GaN-on-Si half-bridge with integrated gate driver chip. Input voltage is 5 V, output voltage is 0.8 V. Switching frequency is 400 kHz, load current is 4.5 A.

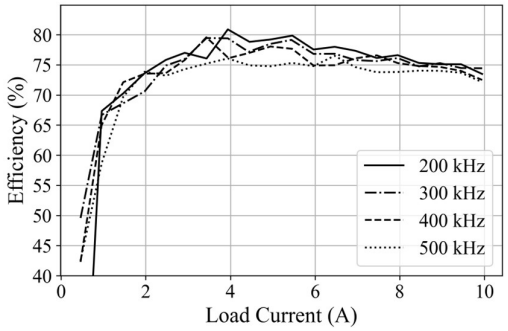

Fig. 8. Efficiency of the half-bridge with integrated gate drivers for various load currents and input frequencies. The input voltage is 5 V, and the output voltage is 0.8 V.

generating an output of 0.8 V from an input of 5 V. The HS and LS gate signals and output signal are depicted. The same configuration is used for generating converter efficiency plots as shown in Fig. 8. The operating frequency is swept from 200 kHz to 500 kHz. A maximum of 80 % overall efficiency is observed. The measurements indicate that 12 % of the power is lost in the output stage, which is 8 % more than expected from simulations using typical values for this technology. This difference is due to the higher effective on-resistance of the half-bridge HEMTs and output capacitance than the simulated values.

VI. Application

Due to the issues with the production of the GaN IC and the timeline, discrete GaN HEMTs were used to test the functionality of the digital controller of the multi-phase approach in addition to the discrete inductor designed to meet the specifications of the converter. A digitally controlled multi-phase buck converter, as shown in Fig. 9, is designed, and tested. The control scheme is based on average current mode control with current sharing logic to prevent overstressing of phases during steady state and transients. Fig. 10 shows the efficiency of the buck converter using one phase only when converting input of 12 V to output of 5 V for various load currents from 1 A to 20 A. It can be noted that an efficiency of around 98 % can be achieved at the operating frequency of 250 kHz. Fig. 11 shows the current sharing waveform at 30 A. It can be noted that two phases share the current equally, which is critical in multi-phase converters for thermal management, overall efficiency, and reliability. Fig. 12 shows the load step response for a current jump from 0 to 20 A, the output voltage moves by less than 1 V and recovers in less than 250 µs. During this load step, Fig. 13 shows the current sharing between the phases. Even during load jumps, the phase inductors share the load current equally. The equal current sharing demonstrates the effective performance of the phase inductors in combination with the digital controller in balancing the load proving the concept.

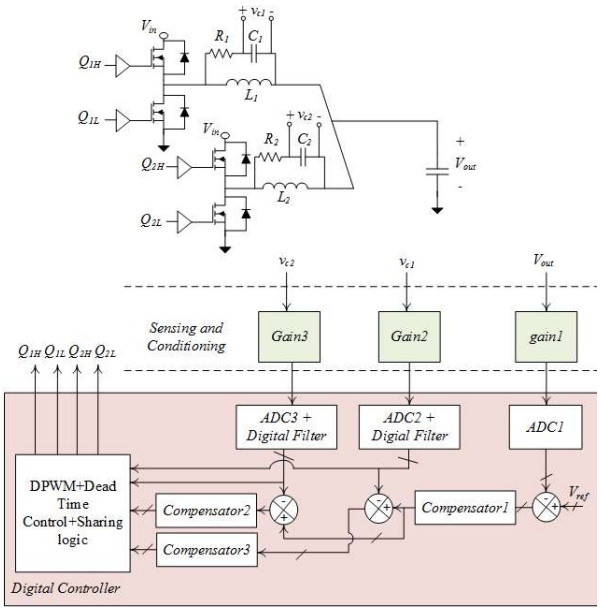

Fig. 9. Block diagram of the two-phase buck converter.

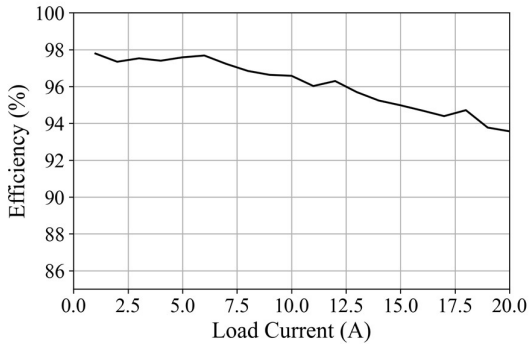

Fig. 10. Efficiency of one phase converting 12 V input to 5 V output at 500 kHz.

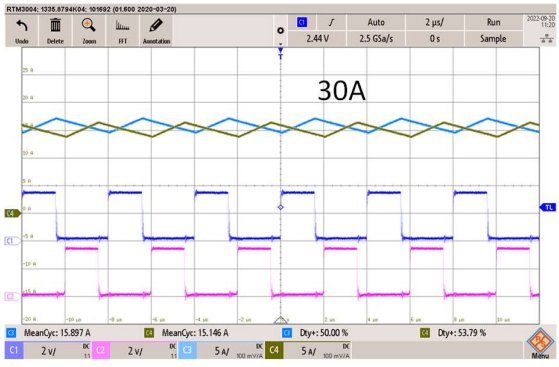

Fig. 11. Current sharing and gating pulses of the two phases at 12 Vin, 5 Vout, 250 kHz and 30 A output current. Light blue and yellow are phases inductor currents and blue and pink are gating pulses for the high side switch for both phases.

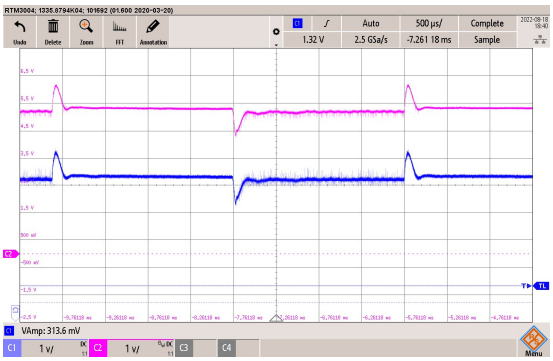

Fig. 12. Load step response for a current jump from 0 A to 20 A, pink and blue are output voltage at different locations on board.

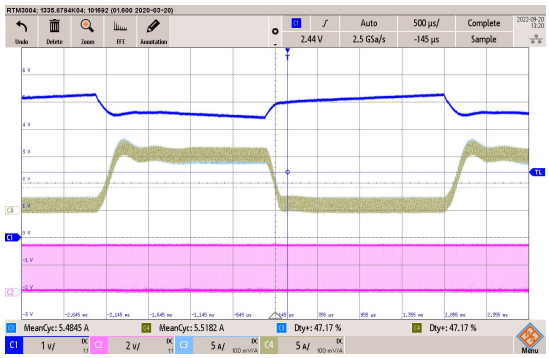

Fig. 13. Current sharing during load jumps. Yellow and light blue are inductor currents.

VII. CONCLUSIONS

In this study, in-depth analysis and comparison of half-bridge ICs developed in 100 V-rated GaN-on-Si and GaN-on-SOI technologies are presented. Through characterization of the ICs, and step-stress testing the two technologies are compared. A quantitative comparison between the technologies demonstrated that the two technologies perform quite closely to each other with GaN-on-Si showing less spread than GaN-on-SOI with lower mean on-resistance. This makes the GaN-on-Si option more interesting for the IC design in terms of higher achievable efficiency.

Furthermore, the investigation into the reliability of the GaN-on-Si half-bridge chips through step stress testing showed that the drain leakage current decreased over time with V_{ds} testing. Gate leakage measurements showed recovery after getting close to the break-down voltage. Very few devices got broken due to V_{ds} testing whereas all devices got broken during V_{gs} testing. This points the importance of proper design techniques such as the use of ESDs and voltage clamps for protecting the gate of the devices in this technology.

In addition, the design and measurement results of a monolithic integrated half-bridge featuring on-chip gate drivers, level shifters, dead time control, and dedicated floating supplies are presented. The circuit's operation is successfully demonstrated in a PoL converter configuration following showing higher chip level integration in the wide bandgap technology compared to multi-chip hybrid Si-GaN counterparts.

Furthermore, a new discrete inductor and a digital controller for a multi-phase approach are tested proving the performance in the functionality testing and highlighting a practical application where the monolithic GaN IC could effectively be used.

ACKNOWLEDGMENT

This activity was supported by the EU-funded GaN Transistor Integrated Circuits project EleGaNT — SPACE-10-TEC-2018-2020. This European co-funded innovation project that has been granted by the ECSEL Joint Undertaking (JU) under grant agreement No 101004274, aimed to improve the level of integration and design in GaN-IC

The authors would like to thank S. Belmans, V. Schillemans for their contributions.

REFERENCES

[1] A. Lidow, J. Strydom, M. de Rooij, and D. Reusch, GaN Transistors for Efficient Power Conversion, 2nd ed., Wiley, Chichester, 2015.

[2] E.Fabris et al.,"Vertical stack reliability of GaN-on-Si buffers for low-voltage applications", 2021 IEEE International Reliability Physics Symposium (IRPS), doi: 10.1109/IRPS46558.2021.9405097.

[3] A. Benato et al., "Scaling of E-mode power GaN-HEMTs for low voltage/low Ron applications: Implications on robustness", vol. 150 (115133), Microelectr. Real. 2023, doi.org/10.1016/j.microrel.2023.115133.

[4] M. Millesimo et al., "The Role of Frequency and Duty Cycle on the Gate Reliability of p-GaN HEMTs", vol. 43, IEEE Electr. Dev. Lett. 2022, doi: 10.1109/LED.2022.3206610.

[5] M. Millesimo et al., "Gate Reliability of p-GaN Power HEMTs Under Pulsed Stress Condition", 2022 IEEE International Reliability Physics Symposium (IRPS), doi: 10.1109/IRPS48227.2022.9764592.

[6] T. Huesgen, "Printed circuit board embedded power semiconductors: A technology review", Power Electronic Devices and Components 3 (2022) 100017